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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/855,641	05/15/2001	Jeremy E. San	1248-29	1734

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EXAMINER	
FOULADI SEMNANI, FARANAK	
ART UNIT	**PAPER NUMBER**
2674	

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/855,641	SAN ET AL.	
	Examiner	Art Unit	
	Faranak Fouladi	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *80-223* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *80-223* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/01, 11/02, 6/03*, 6/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to communications: application, field on 05/15/2001; Preliminary Amendment A, field on 05/15/2001; IDS, paper # 3, received 11/29/02; IDS, paper # 4, received 06/12/03; IDS, paper # 5, received 06/04/04; IDS, paper # 7, received 07/17/01 and supplemental pre-amendment B, received 07/17/01.
2. Claims 80-223 are pending in the case, with claims 80, 98, 117, 135, 154, 172, 186, 187, 202, 204 and 206 being independent.
3. The present title of the application is "**External memory system having programmable graphics processor for use in a video game system or the like**" (as originally field).
4. This application is a continuation of Application No. 08/725,561, field November 30, 2000 (now U.S. Patent No. 6,646,653).

Double Patenting

- The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

  A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 80, 98 and 206 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over U.S. Patent No. 6,646,653.

6. Claim 80 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 and 4 of U.S. Patent No. 6,646,653. Although the conflicting claims are not identical, they are not patentably distinct from each other. From the below side-by-side comparison it is clear that pending claim 80 is broader.

Claims 80 from application under examination	**Claims 1 and 4 from Patent # 6,646,653**
80. A home video game system for use with a television type monitor display device, said system contained, at least in part, in a housing having an insertion port for receiving a removable memory storage device, comprising: a programmable graphics processor; a main processor that communicates information relating to one or more polygon-based 3D graphic objects to said programmable graphics processor, wherein the graphic processor is programmed to render at least one or more portions of said 3D polygon-based graphic objects for display on said display device.	1. An information processing system including a display and a first processing unit for executing at least a first portion of a video graphics program, said video graphics program being received from an external source, and including a second portion having instructions relating to 3-D graphics operations, and a programmable graphics processor separate from said first processing unit comprising: means for receiving instructions from said second portion of said video graphics program; and means for executing said instructions from said second portion of said video graphics program, whereby said graphic processor coacts with first processing unit to control 3-D display of an object. 4. An information processing system according to claim 1, wherein external source comprises an external memory.

Claims 1 and 4 from patent # 6,646,653 include a display, first processing unit for executing at least a first portion of video graphics program and a programmable graphics processor that coacts with first processing unit to control 3-D display of an object. Claim 80 of the present application includes a programmable graphics processor and a main processor that communicates with the programmable graphics processor. Therefore conflicting claims are not patentably distinct from each other.

7. Claim 98 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1,2 and 4 of U.S. Patent No. 6,646,653. Although the conflicting claims are not identical, they are not patentably distinct from each other.

   Claim 98 from the present application broadly claims a game program processing unit and a programmable graphics processor that processes pixel data for rendering 3D objects for display. Similarly, claims 1, 2 and 4 from patent # 6,646,653 include a display, first processing unit for executing at least a first portion of video graphics program and a programmable graphics processor that coacts with first processing unit to process pixel data and to control 3-D display of an object. Therefore the conflicting claims are not patentably distinct from each other.

Claim 98 from application under examination

98. A home video game system for use with a television type monitor display device, said system contained, at least in part, in a housing having an insertion port for receiving a removable memory storage device, comprising:

a game program processing unit for executing at least a portion of a video graphics program for displaying polygon-based 3D objects; and

a programmable graphics processor unit connected to the game program processing unit for receiving information relating to one or more polygon-based 3D graphic objects, the graphics processor programmed to process pixel data for rendering one or more portions of polygon-based 3D objects for display on said television type monitor display.

Claims 1, 2 and 4 from Patent # 6,646,653

1. An information processing system including a display and a first processing unit for executing at least a first portion of a video graphics program, said video graphics program being received from an external source, and including a second portion having instructions relating to 3-D graphics operations, and a programmable graphics processor separate from said first processing unit comprising:

means for receiving instructions from said second portion of said video graphics program; and

means for executing said instructions from said second portion of said video graphics program, whereby said graphic processor coacts with first processing unit to control 3-D display of an object.

2. An information processing system according to claim 1, wherein said means for executing includes circuitry for converting pixel-based format data into character-based format data.

4. An information processing system according to claim 1, wherein external source comprises an external memory.

8. Claim 206 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 and 4 of U.S. Patent No. 6,646,653. Although the conflicting claims are not identical, they are not patentably

distinct from each other. From the below side-by-side comparison it is clear that pending claim 206 is broader.

Claims 206 from application under examination	**Claims 1 and 4 from Patent # 6,646,653**
206. A home video game system for use with a television type monitor display device, said system contained, at least in part, in a housing defining an insertion space for receiving a potable removable non-volatile memory storing instructions and data relating to one or more polygon-based 3D graphic objects, comprising: a programmable graphics processor; and a main processor that accesses said instructions and data and communicates information relating to one or more polygon-based 3D graphic objects to the programmable graphics processor, wherein the graphic processor is programmed to render at least one or more portions of said 3D polygon-based graphic objects for display on said display device.	1. An information processing system including a display and a first processing unit for executing at least a first portion of a video graphics program, said video graphics program being received from an external source, and including a second portion having instructions relating to 3-D graphics operations, and a programmable graphics processor separate from said first processing unit comprising: means for receiving instructions from said second portion of said video graphics program; and means for executing said instructions from said second portion of said video graphics program, whereby said graphic processor coacts with first processing unit to control 3-D display of an object. 4. An information processing system according to claim 1, wherein external source comprises an external memory.

Claims 1 and 4 from patent # 6,646,653 include a display, first processing unit for executing at least a first portion of video graphics program and a programmable graphics processor that coacts with first processing unit to control 3-D display of an object. Claim 206 of the present application includes a programmable graphics processor and a main processor that communicates with the programmable graphics processor. Therefore the conflicting claims are not patentably distinct from each other.

Claim Objections

9. Claims 80 – 86, 88, 90-96, 98-105, 107, 109-115, are objected to because of the following informalities:

   for example, in claim 80 line 7, "wherein the graphics processor" should be changed to " wherein the programmable graphics processor" for consistency. Appropriate correction is required.

10. Claim 138 is objected to because of the spelling error in line 2. The word "assess" should be "access".

11. Claim 202 is objected to because in line 7 "an object" is grammatically wrong and it should read "object", and in line 9 "to" should be added before "a video display RAM".

Claim Rejections - 35 USC § 112

♦ **The following is a quotation of the first paragraph of 35 U.S.C. 112:**

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

12. Claims 85, 88, 92, 98-205, 207, 214 and 218 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

13. Regarding claims 98, 135, 154, 186, the specification does not disclose a game program-processing unit for executing at least a portion of a video graphics program for displaying polygon-based 3D objects.

14. Regarding claims 117, 172, 187, 202, 204 the specification does not disclose a game program processor.

15. Regarding claims 85, 103, 122-124, 141, 154, 174 and 192, the specification does not disclose a graphic processor including graphics geometry transformation circuitry for performing rotation and or scaling of a 3D graphic object or portions of the object to be displayed. The specification does not disclose what the graphics geometry transformation circuitry is or what it includes.

16. Regarding claims 88, 107, 125, 144, 162, 176, 195, 214, the specification does not disclose an array of data corresponding to polygon vertex points that are rotated by programming the graphics processor.

17. Regarding claims 92, 111, 129, 148, 166, 180, 199, and 218, the specification does not disclose a home video game system including a set of instructions for programming the graphics processor unit for rendering 3D objects. What does this set of instructions include?

18. Regarding claim 117, the specification does not disclose the graphics processor including a programmable processor having embedded RAM cache memory.

19. Regarding claim 118, the specification does not disclose what are the specific instructions used for rendering 3D objects that the coprocessor is responsive to?

20. Claims 99-102, 104-106, 108-110, 112-116, 119-121, 126-128, 130-134, 137-140, 142, 143, 145-147, 149-153, 156-161, 163-165, 167-171, 175, 177-179, 181-185, 189-191, 193, 194, 196-198, 200, 201, 203 and 205 incorporate the problems of independent claims 98, 117, 135, 154, 173, 186, 187, 202 and 204 by pendency.

- **The following is a quotation of the second paragraph of 35 U.S.C. 112**:

  The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

21. Claims 159 and 211 recites the limitation "the circuitry" in line 1. There is insufficient antecedent basis for this limitation in the claims.

Claim Rejections - 35 USC § 103

- The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

- **Claims 80, 135 and 206 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5,016,876 to Loffredo in view of US Patent 5,190,285 to Levy et al., hereafter "Levy".**

22. Regarding independent claim 80, "A home video game system for use with a television type monitor display device, said system contained, at least in part, in a housing having an insertion port for receiving a removable memory storage device, comprising:

a programmable graphics processor; (Loffredo disclose in col. 4 lines 50-60 and in Fig. 1 as "a digital computer 22")

a main processor that communicates information relating to one or more polygon-based 3D graphic objects to said programmable graphics processor, (Loffredo disclose in Fig. 1 as "DMA coprocessor 130")

wherein the graphic processor is programmed to render at least one or more portions of said 3D polygon-based graphic objects for display on said display device (Loffredo disclose in col. 9 lines 23-38 and also in col. 1 lines 50-60).
Loffredo does not explicitly disclose removable memory storage device. Levy discloses in col. 6 lines 21-23 a game system that includes a game processor 80, in col. 7 lines 11-14 graphics processor 94 and in col. 6 lines 42-47 an external unit 92. It would have been obvious to one of ordinary skill in the art at the time of invention to substitute the memory storage of Loffredo with the removable memory as taught by Levy to improve the video game by permitting existing processors to address a larger program memory address space.

23. Independent claim 135 is rejected under the same rationale as independent claim 80 above; further the limitation "Video RAM" is disclosed by Loffredo in col. 6 lines 13-21.

24. Independent claim 206 is the same as claim 80, therefore is rejected under the same rationale.

♦ **Claims 81-134, 136-205, 207-223 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5,016,876 to Loffredo in view of US Patent 5,190,285 to Levy et al., hereafter "Levy" and further in view of "PC TECH JOURNAL, "Custom-Tailored Graphics: TMS 34010, by Ed McNierney, July 1987, Pages 68-74; hereafter McNierney.**

25. Regarding claims 81, 99, 118, 136, 155, 173, 188 and 207 the combination of Loffredo with Levy teaches the claimed invention. Furthermore Loffredo discloses in col. 4 lines 49-62 "Texas Instruments Graphics System Processor TMS34010 ("GPS")" but does not disclose the internal architecture of the GPS and therefore the TMS34010's ability to respond to specific instructions used for rendering 3D objects are not clearly disclosed. However, McNierney discloses in page 68-74 TMS34010 "GPS" internal architecture that includes a coprocessor that has a highly pipelined internal architecture, a high-speed arithmetic logic unit and programmable 256-byte instruction cache and a 32 bit barrel shifter that allows it to fetch instructions in parallel with executing instructions and accessing registers and local memory. responsive to specific instructions used for rendering 3D objects.

It would have been obvious to one of ordinary skill in the art at the time of invention to refer, use and rely on McNierney's discloser to illustrate TMS34010 GPS's ability to respond to specific instructions (transformation, clipping and lighting

of the initial object) used for rendering 3D objects and thus illustrating Loffredo's system ability to be responsive to 3D rendering instructions.

26. Regarding claims 82-96,100-115, 119-133, 137, 149, 156-170, 174-184, 189- 201, 208-222; the combination of Loffredo with Levy teaches the claimed invention. Further McNierney discloses in page 68 last column last paragraph TMS34010 that is a pipelined processor and includes an Arithmetic Logic Unit, barrel shifter (multiplier unit that performs multiply operation using at least 16-bit length, a cache RAM and plurality of registers and also is capable of performing graphics-intensive tasks like rotation or scaling of polygon based objects. In addition the GPS TMS34010 include the pixel plotting circuit (McNierney page 68-70), and it includes a set of instructions (McNierney page 71) an instruction for texture mapping and an instruction for controlling transparency of display object and an instruction for fractional signed multiply instruction are included in the set (McNierney page 73). McNierney also discloses in page 71 Fig. 2 that graphics processor incorporates an Arithmetic Logic Unit, cache Ram, high speed multiplier and plurality of registers fabricated on a single chip.

27. Regarding claims 97, 116, 134, 153, 171, 185 and 223, "...further comprising a CD ROM reader device..." Loffredo does not explicitly disclose a CD ROM reader device. Levy discloses a game system that includes a game processor 80, graphics processor 94 and external unit 92 (Levy discloses in col. 10 lines 58-66 "a program memory detachably connected to the main processor for storing program data

associated with an activity to be simulated by the main processor, ..., and program instructions for execution by the main processor for causing the main processor to simulate an activity"); a program memory detachably connected to the main processor may be a CD ROM storage systems that are well known to those skilled in the art.

It would have been obvious to one of ordinary skill in the art at the time of invention to substitute the memory storage of Loffredo with the removable memory as taught by Levy to improve the video game by permitting a different game memory with instructions and data for a different game to be substituted.

28. Regarding independent claim 98, the combination of Loffredo with Levy teaches the claimed invention as discussed in independent claim 80's rejection above. Furthermore, Loffredo discloses in col. 5 line 54- col. 6 line 67 and in col. 9 lines 23-31 pixel processing by the programmed graphics processor (Also this limitation is disclosed by McNierney in page 68 last column lines 5-8).

29. Regarding independent claim 117, the combination of Loffredo with Levy teaches the claimed invention as discussed in independent claim 80's rejection above. Furthermore McNierney discloses in page 71 Fig. 2 and 3 a programmable processor having embedded RAM cache memory.

30. Regarding claims 138, 203 and 205, Loffredo discloses in col. 3 lines 24-27 DMA transfer of pixel data to video RAM.

31. Regarding independent claim 154, the combination of Loffredo with Levy teaches the claimed invention as discussed in independent claim 80's rejection above. Furthermore, McNierney discloses in page 68 last column, last paragraph a graphics processor including an Arithmetic Logic Unit and geometry transformation circuitry.

32. Regarding independent claim 172, the combination of Loffredo with Levy teaches the claimed invention as discussed in independent claim 80's rejection above. Furthermore, McNierney discloses in page 68 last column-page 70 first column a programmable pipelined processor having an Arithmetic Logic Unit, barrel shifter (multiplier unit), a cache RAM and plurality of registers and further discloses that the TMS34010 performs graphics-intensive tasks and since image rotation or scaling on polygon based objects is one of graphics-intensive tasks therefore TMS34010 performs them as well.

33. Regarding independent claims 186, 202 and 205, the combination of Loffredo with Levy teaches the claimed invention as discussed in independent claims 135 and 172's rejection above. Furthermore, McNierney discloses in page 70 the first and second column computing display screen position coordinates for the rotated/or scaled polygon-based object; further Loffredo teaches in col. 5 line 54- col. 6 line 25 writing pixel color information corresponding to the rotated/ or scaled polygon-based object to the video RAM and further

Conclusion

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Faranak Fouladi** whose telephone number is **(571) 272-7689**. The examiner can normally be reached on Mon-Fri from 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Patrick Edouard** can be reach at **(571) 272-7603**.

Any response to this action should be mailed to:

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is **(571) 272-2600**.

Faranak Fouladi

Patent Examiner
Art Unit 2674
June 01, 2005

PATRICK N. EDOUARD
SUPERVISORY PATENT EXAMINER